REMARKS

Applicant appreciates the Examiner's thorough consideration provided the present application. Claims 1-15 are present in the application. Claims 1, 2 and 11 are independent. Reconsideration of this application is respectfully requested.

Allowable Subject Matter

The Examiner has indicated that claims 2-4 and 10 are allowed. The Examiner has also indicated that dependent claims 6-9 and 12-15 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims. Applicant appreciates the indication of allowable subject matter by the Examiner.

Drawings

The Examiner did not indicate whether or not the formal drawings have been accepted. Since no objection has been received, Applicants assume that the drawings are acceptable and that no further action is necessary. Confirmation thereof in the next Office Action is respectfully requested.

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 5 and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's disclosed conventional art in view of Endres et al., U.S. Patent No. 6,426,972 (referred to as "Endres" hereinafter). This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

Independent claim 1 recites a combination of elements including "a DD error size calculation unit for taking the absolute value of a real part and an imaginary part of the first error calculated from the DD slicer, and summing the absolute value of the real part and the absolute value of the imaginary part of the first error to obtain a sum".

Independent claim 11 recites a combination of elements including "fourth means for taking the absolute value of a real part and an imaginary part of the DD error calculated from the second means, and summing the absolute value of the real part and the absolute value of the imaginary part of the DD error to obtain a sum".

Applicant respectfully submits that the combinations of elements as set forth in independent claims 1 and 11 are not disclosed or suggested by references relied on by the Examiner.

The Examiner relied on Applicant's disclosed conventional art to reject claims 1, 5 and 11 under 35 U.S.C. § 103(a), which is inappropriate because at the outset, no admission had been made by Applicant that Applicant's disclosed conventional art qualifies as statutory prior art usable in a rejection of the claim of the instant application. Instead, Applicant has labeled FIGs. 1 and 2 as "Conventional Art" to distinguish Applicants' invention from that which is not Applicants' invention. At least for this reason, Applicant respectfully requests that this rejection be withdrawn.

In the alternative, as the Examiner correctly indicated, Applicant's disclosed conventional art fails to teach "a DD error size calculation unit for taking the absolute value of a real part and an imaginary part of the first error calculated from the DD slicer, and summing the absolute value of the real part and the absolute value of the imaginary part of the first error to obtain a sum" as recited in claim 1 and "fourth means for taking the absolute value of a real part and an imaginary part of the DD error calculated from the second means, and summing the absolute value of the real part and the absolute value of the imaginary part of the DD error to obtain a sum" as recited in claim 11. To correct this deficiency of Applicant's disclosed conventional art, the Examiner turned to rely on Endres's absolute value circuits 516 and 518 in FIG. 5 and alleged that the combination of Applicant's disclosed conventional art and Endres's absolute value circuits 516 and 518 teaches the above combinations of elements as recited in claims 1 and 11. Applicant respectfully disagrees.

Endres discloses that the absolute value circuits 516 and 518 provide the magnitudes of the respective I and Q components of *the coefficient value of the sparse filter* to an adder 517 (see col. 12, lines 48-53). However, the I and Q components of the coefficient values of the *sparse filter* are not the real part and an imaginary part of *the first error calculated from the DD slicer* as recited in claim 1 or the real part and an imaginary part of the *DD error calculated from the second means* as recited in claim 11. In fact, Endres's I and Q components are the filter tap coefficients of the spare filter such as the FIR filter 216 and IIR filter 230 used in the equalizer (see FIGs. 2A-2C; col. 9, col. 57-61).

Endres nowhere discloses taking the absolute value of a real part and an imaginary part of *the first error (or DD error)* as required by the independent claims. Thus, Endres fails to cure the deficiencies of Applicant's disclosed conventional art.

Further, there is no motivation to modify Applicant's disclosed conventional art to arrive at the claimed invention, since the specific mathematical operation taught by Endres is applied to the filter tap coefficients and not to the first error calculated from the DD slicer (or DD error), as required by the independent claims.

Accordingly, neither Applicant's disclosed conventional art nor Endres individually or in combination teaches or suggests at least the above-noted features of independent claims 1 and 11. Therefore, Applicant respectfully submits that independent claims 1 and 11 and dependent claim 5 (due to its dependency from independent claim 1) clearly define over the teachings of Applicant's disclosed conventional art and Endres. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103 are respectfully requested.

Additional Cited References

Since the remaining patents cited by the Examiner have not been utilized to reject the claims, but rather to merely show the state of the art, no further comments are necessary with respect thereto.

CONCLUSION

All the stated grounds of rejection have been properly traversed and/or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently pending rejections and that they be withdrawn.

It is believed that a full and complete response has been made to the Office Action, and that as such, the Examiner is respectfully requested to send the application to Issue.

In the event there are any matters remaining in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

Applicant respectfully petition under the provisions of 37 C.F.R. § 1.136(a) and § 1.17 for a one-month extension of time in which to respond to the Examiner's Office Action. The Extension of Time Fee in the amount of $ 120.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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